REMARKS

Claims 1-31, 97, and 98 are pending in the present application. Claims 1, 97, and 98 have been amended. A marked-up version of this claim, showing changes made, is attached hereto as Appendix A. Applicants respectfully request reconsideration of all rejections in light of the amendments and following remarks.

Applicants also include a "Request for Continued Examination" filed concurrently herewith to expedite prosecution of the above-referenced patent application.

Claim 97 stands rejected under 35 U.S.C. § 112, second paragraph, as lacking proper antecedent basis. Claim 97 has been amended to include proper antecedent basis. Specifically, Claim 97 now recites "an annealed platinum layer formed over said tantalum pentoxide layer." Thus, withdrawal of this rejection is respectfully requested.

Claims 1-31 and 98 stand rejected under 35 USC §102 as being anticipated by Agarwal et al. (U.S. Patent No. 6,297,527) ("Agarwal"). Reconsideration is respectfully requested.

The claimed invention relates to a capacitor structure with an annealed top conducting layer. As such, independent claim 1 recites a "capacitor for a semiconductor device . . . comprising a bottom conducting layer, a dielectric layer formed over said bottom conducting layer, and an annealed oxygen permeable top conducting layer formed over said dielectric layer." (emphasis added). Similarly, claim 98 recites a "capacitor for a semiconductor device . . . comprising a bottom conducting layer, a dielectric layer formed over said bottom conducting layer, and an annealed top conducting layer formed over said dielectric layer . . . ." (emphasis added).

Agarwal merely relates to a capacitor structure with "an upper electrode 70, a dielectric layer 72, and a lower electrode having multiple layers." (Col. 5, lines 15-17). According to Agarwal, the upper electrode 70 "may be a single layer of suitable conductive material . . . or may have a multilayer structure identical to that of the lower electrode, with

a platinum layer and a platinum-rhodium layer." (Col. 6, lines 49-54; Figure 2). Further, Agarwal teaches that "CVD, PVD, sputtering, evaporation, or other suitable means may be used to *form* the upper electrode." (Col. 6, lines 54-55; Figure 8) (emphasis added).

The Office Action contends that Agarwal teaches "an oxygen permeable top conducting layer 70 formed by *plasma enhanced annealed layer*" (Office action, page 3) (emphasis added). Applicants do not understand this assertion and respectfully disagree.

Agarwal simply does not teach or suggest a capacitor comprising "an *annealed* oxygen permeable top conducting layer formed over said dielectric layer," as independent claim 1 recites (emphasis added), nor a capacitor comprising "an *annealed* top conducting layer," as independent claim 98 recites (emphasis added). Agarwal is completely silent about an *annealed* upper conducting layer as recited by independent claims 1 and 98. Agarwal's Figure 8 (Col. 6, lines 48), Figure 14 (Col. 7, lines 18-22), and Figure 21 (Col. 7, lines 53-56) are completely void of any discussion of an annealed top conducting layer as recited by independent claims 1 and 98.

For at least the reasons described above, dependent claims 2-32 which depend from and incorporate all of the limitations of claim 1, are similarly allowable.

Claim 97 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Agarwal et al. in view of Applicants' cited reference, Lai et al ("Lai"). Reconsideration is respectfully requested.

The cited references, alone or in combination, fail to teach or suggest the subject matter of claim 97.

For similar reasons stated above, Agarwal does not teach or suggest a capacitor comprising an annealed top conducting layer, much less, an "*annealed platinum layer* formed over said dielectric layer," as independent claim 97 recites (emphasis added).

Further, Agarwal and Lai are directed to solving different problems. Agarwal

provides an "*improved lower electrode* for a ferroelectric or high dielectric constant capacitor having the advantages of a platinum electrode while avoiding problems of oxidation and separation from the substrate." (Col. 3, lines 17-20) (emphasis added). Whereas, Lai is directed to studying the reduction of leakage current in PECVD and LPCVD deposited Ta_2O_5 films (Lai, page 1, Col. 1).

Accordingly, even assuming arguendo that the cited references are combinable, which they are not, one still would not obtain the present invention. The cited references fail to teach or suggest a capacitor for a semiconductor device comprising "a tungsten nitride bottom layer, a tantalum pentoxide layer formed over said tungsten nitride layer bottom layer, and an *annealed platinum layer* formed over said dielectric layer," as independent claim 97 recites (emphasis added).

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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APPENDIX A

1. (amended) A capacitor for a semiconductor device, said capacitor comprising:

a bottom conducting layer;

a dielectric layer formed over [deposited on] said bottom conducting layer; and

an annealed oxygen permeable top conducting layer formed over [deposited and annealed on] said dielectric layer.

97. (amended) A capacitor for a semiconductor device, said capacitor comprising:

a tungsten nitride bottom layer;

a tantalum pentoxide layer formed over said tungsten nitride bottom layer; and

an annealed platinum layer formed over said tantalum pentoxide [dielectric] layer.

98. (amended) A capacitor for a semiconductor device, said capacitor comprising:

a bottom conducting layer;

a dielectric layer formed over said bottom conducting layer; and

an annealed top conducting layer formed over said dielectric layer, wherein each of said bottom and annealed top conducting layers is formed of a material selected from the group consisting of platinum, platinum rhodium, platinum iridium, and tungsten nitride.